REMARKS

Claims 48-49, 51-56, 59-65, and 68-69 remain in this application. No claims have been added, cancelled, or amended. The Applicants respectfully request reconsideration of this application in view of the above amendments and the following remarks.

35 U.S.C. §102(b) Rejection – Shields

The Examiner has rejected claim 48 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,350,696 issued to Shields et al. (hereinafter referred to as "Shields"). The Applicants respectfully submit that claim 48 is not anticipated by Shields.

Claim 48 recites a method comprising "*forming insulating spacers adjacent to sidewalls of a gate by forming an insulating layer and removing a portion of the insulating layer that is not on the sidewalls including performing a combination of a dry etch and then a wet etch; and forming extension regions after forming the insulating spacers by ion implantation using the insulating spacers as a mask*".

Shields does not teach or reasonably suggest that the spacers 710 are used to form extension regions. In fact, Shields does **not even mention extension regions or forming extension regions**. Shields discusses source and drain. At column 1, lines 15-23 it is stated "*In integrated circuits having transistors, for example, one very important process step is the formation of the gate, **source**, and **drain** regions for each of the transistors and, in particular, the dimensions of the gate, source, and drain regions. Often, the performance characteristics (e.g., switching speed) and size of the transistor are functions of the size.(e.g., width) of the transistor's gate, and the **placement of the source and drain regions***". As further discussed at column 1, lines 31-33 "*spacers are used in*

conventional semiconductor devices ***to provide alignment of the source and drain regions*** *to the gates in transistors*". Now, extension regions are well known in the arts and are known to be different than source and drain. Accordingly, Applicants submit that the spacers are instead to form the source and the drain not extension regions.

Anticipation under 35 U.S.C. Section 102 requires every element of the claimed invention be identically shown in a single prior art reference. The Federal Circuit has indicated that the standard for measuring lack of novelty by anticipation is **strict identity**. "For a prior art reference to anticipate in terms of 35 U.S.C. Section 102, every element of the claimed invention must be identically shown in a single reference." In Re Bond, 910 F.2d 831, 15 USPQ.2d 1566 (Fed. Cir. 1990).

Accordingly, claim 48, and its dependent claims, are believed to be allowable.

35 U.S.C. §102(b) Rejection – Lowrey

The Examiner has rejected claim 48 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,032,530 issued to Lowrey et al. (hereinafter referred to as "Lowrey"). The Applicants respectfully submit that claim 48 is not anticipated by Lowrey.

As clearly shown in FIG. 7 of Lowrey the heavily doped N+ regions 72 are not the claimed extension regions recited in claim 48. Accordingly, claim 48, and its dependent claims, are believed to be allowable.

35 U.S.C. §102(b) Rejection – Kwon

The Examiner has rejected claims 61 and 63 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,424,234 issued to Kwon et al. (hereinafter referred to as

"Kwon"). The Applicants respectfully submit that the present claims are allowable over Kwon.

Claim 61 recites a method comprising "*forming insulating spacers adjacent to sidewalls of a gate; forming extension regions after forming the insulating spacers by ion implantation using the insulating spacers as a mask; removing the insulating spacers by etching; and forming a source and a drain by ion implantation*".

Kwon does not teach or reasonably suggest forming **extension regions** after forming the insulating spacers by ion implantation using the insulating spacers as a mask. As stated at column 4, lines 10-11, what the Examiner has referred to as extension regions are in fact not extenuation regions but rather "***N+ type source and drain regions 8 and 8a***". As discussed above, source and drain are not extension regions.

Anticipation under 35 U.S.C. Section 102 requires every element of the claimed invention be identically shown in a single prior art reference. The Federal Circuit has indicated that the standard for measuring lack of novelty by anticipation is **strict identity**. "For a prior art reference to anticipate in terms of 35 U.S.C. Section 102, every element of the claimed invention must be identically shown in a single reference." In Re Bond, 910 F.2d 831, 15 USPQ.2d 1566 (Fed. Cir. 1990).

Accordingly, claim 61, and its dependent claims, are believed to be allowable.

35 U.S.C. §103(a) Rejection – Shields in view of Wolf

The Examiner has rejected claims 53-54, 56 and 59-60 under 35 U.S.C. §103(a) as being unpatentable over Shields as applied to claims 51-52 above and further in view of Wolf et al, "Silicon Processing for the VLSO Era Volume 1: Process Technology" (hereinafter referred to "Wolf"). Without admitting the appropriateness of combining

Shields and Wolf, the Applicants respectfully submit that the present claims are allowable over any combination of Shields and Wolf.

Claim 53 recites a method comprising "*forming insulating spacers adjacent to sidewalls of a gate by depositing an insulating layer at a temperature that is higher than 750°C and anisotropically etching the insulating layer; and forming extension regions after forming the insulating spacers by ion implantation using the insulating spacers as a mask*".

Shields does not teach or suggest forming extension regions using the insulating spacers. The discussion above is pertinent to this point. Wolf does not remedy what is missing in Shields. Accordingly, any combination of Shields and Wolf does not teach or suggest the limitations of claim 53.

Accordingly, claim 53, and its dependent claims, are believed to be allowable.

35 U.S.C. §103(a) Rejection – Lowery in view of Wolf

The Examiner has rejected claims 53-54, 56 and 59-60 under 35 U.S.C. §103(a) as being unpatentable over Lowery as applied to claims 51-52 above and further in view of Wolf. Without admitting the appropriateness of combining Lowery and Wolf, the Applicants respectfully submit that the present claims are allowable over any combination of Lowery and Wolf.

Claim 53 recites a method comprising "*forming insulating spacers adjacent to sidewalls of a gate by depositing an insulating layer at a temperature that is higher than 750°C and anisotropically etching the insulating layer; and forming extension regions after forming the insulating spacers by ion implantation using the insulating spacers as a mask*".

Lowery does not teach or suggest forming extension regions using the insulating spacers. The discussion above is pertinent to this point. Wolf does not remedy what is missing in Lowery. Accordingly, any combination of Lowery and Wolf does not teach or suggest the limitations of claim 53.

Accordingly, claim 53, and its dependent claims, are believed to be allowable.

Conclusion

In view of the foregoing, it is believed that all claims now pending patentably define the subject invention over the prior art of record and are in condition for allowance. Applicants respectfully request that the rejections be withdrawn and the claims be allowed at the earliest possible date.

Request For Telephone Interview

The Examiner is invited to call Brent E. Vecchia at (303) 740-1980 if there remains any issue with allowance of the case.

Request For An Extension Of Time

The Applicants respectfully petition for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17 for such an extension.

Charge Our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: 11-30-05

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